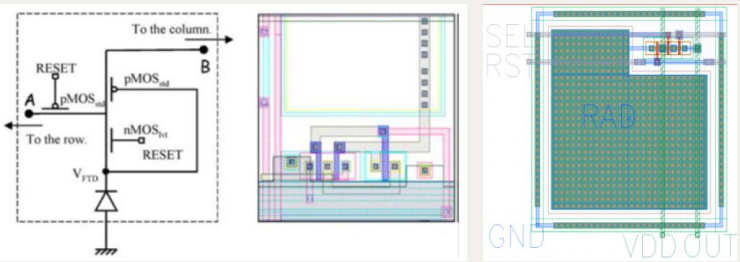
DIPARTIMENTO DI INGEGNERIA
CORSO DI DOTTORATO IN INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE -
PHD COURSE IN INDUSTRIAL AND INFORMATION ENGINEERING - 37TH CYCLE

Title of the research activity:	**Advanced Radiation Sensors and Readout CMOS Architectures for applications in harsh environment** *Research Field*: **Sensors and Electronics, Medical, Space and Physics applications**. *International and National Collaborations*: **CERN** (European Organization for Nuclear Research, Switzerland); **LFoundry** (Avezzano, Italy), **INFN** (Istituto Nazionale di Fisica Nucleare, Italy). *International and National Projects*: CERN RD53 International Collaboration, EU AIDAinnova Horizon Europe, INFN FOOT, ARCADIA projects.
State of the Art:	Present radiation pixel sensors and related read-out electronics forces to face some critical issues in the microelectronics design as follows: - the increased number of read-out channels forces to have more accurate power budget (**reduced power consumption** of each channel). - the increased number of read data forces to develop advanced algorithms for data handling - any integrated circuit will be exposed to **extremely large radiation dose**, up to 1 Grad in 10 years. Optimal IC design is therefore required for high-performance, low-power and low-cost systems. These results can be achieved with a custom design and performance optimization since different experiments and applications require different specifications in terms, for instance, of radiation hardness, power supply, power consumption, accuracy.
Short description and objectives of the research activity:	The purpose of the present research is to exploit innovative CMOS technologies options [Wang-2017, Beckers-2018] in terms of: - minimum gate size (65nm, 45nm, 32nm, 28nm, or below) - technology features (CMOS-bulk, CMOS-FinFET, CMOS-SOI, etc…) - technology access & cost (this is in terms not only of prototyping for investigation, but also for the final production) This will enable: - higher digital circuit density to includes more digital functionalities - higher speed to achieve improved performance in term of larger bandwidth, enabling new application In particular, the main outcome of the project is to develop innovative CMOS monolithic pixel detectors that can replace standard hybrid pixel and silicon strip detectors in a wide range of applications such as High Energy Physics experiments, Medical applications as well as Space applications. The proposed development relies on three key elements: – a **sensor fabrication technology** that, starting from the experience gained in the previous research activity within national and international collaborations and projects, will improve in such a way to be suitable for a wide range of applications. – a set of smaller-size **test structures** to investigate relevant issues that can be addressed without full-size prototypes (e.g. radiation resistance, monitoring of the substrate properties, influence of different pixel's architectures on charge collection efficiency).

	– a **versatile and scalable front-end electronics** and architectures, capable to effectively support the development of sensors with realistic size and performances. The CMOS electronics will be common to the different sensor options, that will be explored by changing only the substrate material and/or some step of the production process. All the design improvements and modifications introduced in the process flow will be validated with the help of Technology Computer-Aided Design (TCAD) simulations, relying on process data provided by the foundry. A proper TCAD modeling of the bulk and surface radiation damage effect should also be devised and validated for the selected technology [*Moscatelli-2016*], thus fostering its application for the comparison of different layout/doping profiles aiming at optimizing the radiation resistance of the device in terms of SNR and breakdown effects. Aiming at low power design, alternative pixel front-end architectures will be investigated [*Placidi-2016*]. A so-called Weak Inversion Pixel Sensor (WIPS), shown in Fig. 1, exploits a dedicated, yet simple circuitry, based on a pre-charge/evaluation scheme, which allows for ‘‘sparse’’ access mode and thus for speeding-up the read-out phase [*Passeri-2004*].  Fig. 1: CMOS WIPS scheme: equivalent circuit (left-hand side), corresponding layout (right-hand side)
Bibliography:	[*Beckers-2018*] A. Beckers et al. “Characterization and Modeling of 28-nm Bulk CMOS Technology Down to 4.2 K”, IEEE Journal of the Electron Devices Society, Year: 2018, Volume: 6 [*Wang-2017*] T. Wang et al., "Development of a Depleted Monolithic CMOS Sensor in a 150 nm CMOS Technology for the ATLAS Inner Tracker Upgrade", JINST 12 (2017) C01039. [*Passeri-2004*] D. Passeri, P. Placidi, M. Petasecca, P. Ciampolini, G. Matrella, A. Marras, A. Papi, G.M.Bilei, “Design, Fabrication, and Test of CMOS Active-Pixel Radiation Sensors”, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 51, NO. 3, JUNE 2004. [*Placidi-2016*] E. Conti, S. Marconi, T. Hemperek, J. Christiansen and P. Placidi, “Performance evaluation of digital pixel readout chip architecture operating at very high rate through a reusable UVM simulation framework”, Proc. of NSS (2016). [*Moscatelli-2016*] F. Moscatelli et al., “Combined Bulk and Surface Radiation Damage Effects at Very High Fluences in Silicon Detectors: Measurements and TCAD Simulations”, IEEE Trans. on Nucl. Sci.63 (5), (2016) 2716-2723.
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